Remarks

Applicant respectfully requests reconsideration of this application. Pending claims 1-29 remain unchanged. No claims have been allowed.

Claim Rejection - 35 U.S.C. § 102(b)

Claims 1-29 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Takiguchi (US 5,986,463; "Takiguchi").

The Office Action states that Takiguchi teaches a buffer for noise rejection in a logic circuit. Applicant respectfully disagrees. Takiguchi merely teaches a differential signal generating circuit 16 coupled to drive a differential switch 18. The differential signal generating circuit 16 includes a plurality of inverters coupled so as to suppress current spikes at the output of the differential switch when operating at high frequency. (Column 2, lines 56-67)

Moreover, Takiguchi fails to teach an input node, an output node, a first inverter coupled to the input node, the first inverter having a first device size, and a second inverter coupled to the first inverter and the output node, the second inverter having a second device size at least six times greater than the first device size, as recited in claim 1. Rather, with respect to his differential signal generating circuit, Takiguchi teaches the size of his inverters 22-24 to be unity, to be 2 for inverter 32, and 3 for inverters 42 and 43. (Col. 1, lines 33-39) In the differential signal generating circuit of Figure 9a, Takiguchi teaches the size of his inverter 32 set to be 2, with the size of inverters 42 and 43 to be 3, and 0.75 for inverters 36 and 55-57. (Column 2, lines 52-55) Hence, there is no teaching of the claimed device sizes in Takiguchi's signal generating circuit.

As to independent claims 5 and 16, Takiguchi fails to teach a "computer-aided method for design of a logic network". Indeed, there is nothing in the Takiguchi reference that comes close to disclosing such a method. For example,

there is no disclosure or teaching in Takiguchi of a computer-implemented method comprising extracting parametric information from a layout of the logic network, analyzing the logic network to identify a crosstalk-induced glitch at a node of a signal path in the logic network, and inserting a buffer at the node that functions to suppress a magnitude of the crosstalk-induced glitch. The same is true with respect to Applicant's claim 24 directed to a computer-readable storage medium.

Because the foregoing discussed elements are missing from the cited prior art reference, Applicant respectfully submits that the subject matter of claims 1-29 is not anticipated by Takiguchi.

Accordingly, Applicant respectfully requests that the rejections of claims 1-29 under 35 U.S.C. § 102(b) be withdrawn.

Please charge any shortages and credit any overcharges to our Deposit Account No. 50-2060.

Respectfully submitted,
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